Day : Tuesday
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Time: 17:04:33

Inventor Name Search Result

Your Search was:

Last Name = LEIPOLD
First Name = DIRK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60771121	Not Issued	20	02/06/2006	Use of divide RF clock with AM modulation capability for power efficient, low spurs, TRP compliant power control loop using a synchronous high frequency switching powers supply and second harmonic synchronous RF loop-back detection in receiver	LEIPOLD, DIRK
09969307	Not Issued	41	10/02/2001	Method and apparatus for asynchronous clock retiming	LEIPOLD, DIRK D.
09312511	6348718	150	05/14/1999	INTEGRATED CMOS CIRCUIT HAVING ACTIVE COMPONENTS FORMED IN A HIGH RESISTIVITY SUBSTRATE WITH A LOW RESISTIVITY CONDUCTIVE LAYER LOCATED UNDERNEATH THE ACTIVE COMPONENTS AND HAVING PASSIVE COMPONENTS FORMED IN OR ON AN INSULATING LAYER	LEIPOLD, DIRK ROBERT WALTER

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = MUHAMMAD
First Name = KHURRAM

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60343784	Not Issued	159	12/28/2001	Clock noise suppression by stopping operation of the sampling-mode mixer	MUHAMMAD, KHURRAM
60343938	Not Issued	159	12/28/2001	Current domain sampling in subsampling communication receiver architecture including filter realization with current steering	MUHAMMAD, KHURRAM
60344262	Not Issued	159	12/28/2001	Current domain sampling in subsampling communication receiver architecture including filter realization with current steering and differential coefficients	MUHAMMAD, KHURRAM
60348902	Not Issued	159	10/26/2001	Current steering approach for placing two zeros on folded-over frequencies in decimating FIR filters	MUHAMMAD, KHURRAM
60356620	Not Issued	159	10/25/2001	Sampled domain passive anti-aliasing FIR filter structure with decimation function	MUHAMMAD, KHURRAM
60389872	Not Issued	159	06/19/2002	Graduated exponential bandwidth shifting of an all-digital PLL	MUHAMMAD, KHURRAM
60411814	Not Issued	159	09/18/2002	Active removal of fractional spurs in an ADPLL	MUHAMMAD, KHURRAM
60441080	Not Issued	159	01/17/2003	Type-II-all-digital PLL in deep-submicron CMOS	MUHAMMAD, KHURRAM
60489453	Not Issued	159	07/23/2003	Method of rate conversion together with I-Q mismatch correction and sampler phase adjustment in direct sampling based down-conversion	MUHAMMAD, KHURRAM

60546249	Not Issued	159	02/19/2004	Clock retiming and synchronization method for noise suppression in the digital radio processor	MUHAMMAD, KHURRAM
60776592	Not Issued	20	02/24/2006	Method for spur cancellation by injecting anti-spur in the power supply system	MUHAMMAD, KHURRAM
60776839	Not Issued	20	02/24/2006	Method for LO leakage cancellation by injecting the canceling RF signal through bondwires	MUHAMMAD, KHURRAM

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** MUHAMMAD **First Name** KHURRAM Search

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Inventor Name Search Result

Your Search was:

Last Name = STASZEWSKI
First Name = ROBERT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
60728402	Not Issued	20	10/19/2005	Built-in self-test method for digitally controlled xtal oscillator (DCXO)	STASZEWSKI, ROBERT B.
60773721	Not Issued	20	02/15/2006	Built-in self test and characterization of an on-chip RF power amplifier	STASZEWSKI, ROBERT B.
60773759	Not Issued	20	02/15/2006	Scheme to achieve precise delay alignment between amplitude and phase/frequency modulation paths in digital polar transmitters and for closed loop two-point modulation at different injection rates in ADPLL	STASZEWSKI, ROBERT B.
60773775	Not Issued	20	02/15/2006	Linearization of an RF power amplifier	STASZEWSKI, ROBERT B.
60774107	Not Issued	20	02/16/2006	Frequency tuning range extension and modulation resolution improvement of a digitally controlled oscillator	STASZEWSKI, ROBERT B.
60823837	Not Issued	20	08/29/2006	Generation of Local-Oscillator Signal with Non-Integer Multiplication Ratio Between the Local-Oscillator and the RF Frequencies	STASZEWSKI, ROBERT B.
07998474	5376847	150	12/30/1992	PHASE DETECTOR AND METHODOLOGY	STASZEWSKI, ROBERT B.
08072311	5508673	150	06/02/1993	HIGH FREQUENCY TRANSFORMER APPARATUS	STASZEWSKI, ROBERT B.
08092592	Not Issued	161	07/16/1993	TRANSFORMER DEVICE AND OPERATION	STASZEWSKI, ROBERT B.
09053867	6037886	150	04/01/1998	METHOD AND APPARATUS FOR EXTRACTING BAND	STASZEWSKI, ROBERT B.

				AND ERROR VALUES FROM DIGITAL SAMPLES OF AN ANALOG SIGNAL	
09060918	6212664	150	04/15/1998	METHOD AND SYSTEM FOR ESTIMATING AN INPUT DATA SEQUENCE BASED ON AN OUTPUT DATA SEQUENCE AND HARD DISK DRIVE INCORPORATING SAME	STASZEWSKI, ROBERT B.
09224364	6243729	150	12/31/1998	DIGITAL FINITE-IMPULSE-RESPONSE (FIR) FILTER WITH A MODIFIED ARCHITECTURE BASED ON HIGH ORDER RADIX-N NUMBERING	STASZEWSKI, ROBERT B.
09247131	6252733	150	02/09/1999	METHOD AND APPARATUS FOR ACQUIRING A PREAMBLE SIGNAL IN A HARD DISK DRIVE	STASZEWSKI, ROBERT B.
09256420	6636572	150	02/24/1999	HIGH-SPEED DIGITAL TIMING AND GAIN GRADIENT CIRCUIT EMPLOYING A PARALLEL ARCHITECTURE	STASZEWSKI, ROBERT B.
09256568	Not Issued	161	02/24/1999	FINITE-IMPULSE-RESPONSE (FIR) FILTER EMPLOYING A PARALLEL ARCHITECTURE	STASZEWSKI, ROBERT B.
09258045	Not Issued	161	02/25/1999	SYSTEM AND METHOD FOR OPTIMIZING SIGNAL PROCESSING VIA A UNIQUE TRUNCATING AND ROUNDING OPERATION	STASZEWSKI, ROBERT B.
09258594	6442197	150	02/26/1999	PHASE-SHIFT CALCULATION METHOD, AND SYSTEM IMPLEMENTING IT, FOR A FINITE-IMPLUSE-RESPONSE (FIR) FILTER	STASZEWSKI, ROBERT B.
09258827	6587529	150	02/25/1999	PHASE DETECTOR ARCHITECTURE FOR PHASE ERROR ESTIMATING AND ZERO PHASE RESTARTING	STASZEWSKI, ROBERT B.
09322671	6191716	150	05/28/1999	HIGH-SPEED DIGITAL CIRCUIT EMPLOYING A BAND-ZERO-	STASZEWSKI, ROBERT B.

				DETERMINATION-ASIDE (B0DA) ARCHITECTURE	
09410510	6618740	150	10/01/1999	METHOD AND ARCHITECTURE FOR CONTROLLING ASYMMETRY OF AN LMS ADAPTATION ALGORITHM THAT CONTROLS FIR FILTER COEFFICIENTS	STASZEWSKI, ROBERT B.
09430385	6523052	150	10/29/1999	METHOD AND ARCHITECTURE TO FACILITATE ACHIEVING A FAST EPR4 EQUALIZATION START-UP IN A MAGNETIC RECORDING READ CHANNEL	STASZEWSKI, ROBERT B.
60122196	Not Issued	159	03/01/1999	METHOD AND ARCHITECTURE TO FACILITATE ACHIEVING A FAST EPR4 EQUALIZATION START-UP IN A MAGNETIC RECORDING READ CHANNEL	STASZEWSKI, ROBERT B.
60122219	Not Issued	159	03/01/1999	HIGH-SPEED CIRCUITS EMPLOYING A BAND-ZERRO-DETERMINATION-ASIDE (B0DA) ARCHITECTURE	STASZEWSKI, ROBERT B.
60122227	Not Issued	159	03/01/1999	METHOD AND ARCHITECTURE OF CONTROLLED ASYMMETRY OF AN LMS ADAPTATION ALGORITHM THAT COTROLS FIR FILTER COEFFICIENTS	STASZEWSKI, ROBERT B.
11015562	Not Issued	30	12/17/2004	Multi-function digital device as a human-input-device for a computer	STASZEWSKI, ROBERT BOGDAN

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** STASZEWSKI **First Name** ROBERT Search

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Inventor Name Search Result

Your Search was:

Last Name = LEIPOLD
First Name = DIRK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09603023	6326851	150	06/26/2000	Digital phase-domain PLL frequency synthesizer	LEIPOLD, DIRK
09608317	6429693	150	06/30/2000	DIGITAL FRACTIONAL PHASE DETECTOR	LEIPOLD, DIRK
09679793	6658748	150	10/05/2000	DIGITALLY-CONTROLLED L-C OSCILLATOR	LEIPOLD, DIRK
09695516	6809598	150	10/24/2000	HYBRID OF PREDICTIVE AND CLOSED-LOOP PHASE-DOMAIN DIGITAL PLL ARCHITECTURE	LEIPOLD, DIRK
09790376	6414555	150	02/22/2001	FREQUENCY SYNTHESIZER	LEIPOLD, DIRK
09798106	Not Issued	120	03/02/2001	Buried layer and method	LEIPOLD, DIRK
09828338	6959049	150	04/06/2001	MULTI-TAP, DIGITAL-PULSE-DRIVEN MIXER	LEIPOLD, DIRK
09838451	6606004	150	04/19/2001	SYSTEM AND METHOD FOR TIME DITHERING A DIGITALLY-CONTROLLED OSCILLATOR TUNING INPUT	LEIPOLD, DIRK
09967275	6593773	150	09/28/2001	POWER SAVING CIRCUITRY USING PREDICTIVE LOGIC	LEIPOLD, DIRK
10001448	Not Issued	41	10/31/2001	Transmit filter	LEIPOLD, DIRK
10006607	6734741	150	11/30/2001	FREQUENCY SYNTHESIZER WITH DIGITALLY-CONTROLLED OSCILLATOR	LEIPOLD, DIRK
10099831	7079826	150	03/15/2002	DIGITALLY CONTROLLED ANALOG RF FILTERING IN SUBSAMPLING COMMUNICATION RECEIVER ARCHITECTURE	LEIPOLD, DIRK

10114227	6882829	150	04/02/2002	INTEGRATED CIRCUIT INCORPORATING RF ANTENNA SWITCH AND POWER AMPLIFIER	LEIPOLD, DIRK
10121761	Not Issued	41	04/12/2002	Sampling mixer with asynchronous clock and signal domains	LEIPOLD, DIRK
10131523	Not Issued	41	04/24/2002	Digital phase locked loop	LEIPOLD, DIRK
10132025	7003276	150	04/25/2002	SUBSAMPLING COMMUNICATION RECEIVER ARCHITECTURE WITH GAIN CONTROL AND RSSI GENERATION	LEIPOLD, DIRK
10132436	6963732	150	04/25/2002	SUBSAMPLING COMMUNICATION RECEIVER ARCHITECTURE WITH RELAXED IFA READOUT TIMING	LEIPOLD, DIRK
10132624	Not Issued	41	04/25/2002	Spread spectrum demodulation using a subsampling communication receiver architecture	LEIPOLD, DIRK
10147784	7006813	150	05/16/2002	EFFICIENT CHARGE TRANSFER USING A SWITCHED CAPACITOR RESISTOR	LEIPOLD, DIRK
10154093	6924681	150	05/22/2002	EFFICIENT PULSE AMPLITUDE MODULATION TRANSMIT MODULATION	LEIPOLD, DIRK
10190867	Not Issued	41	07/08/2002	Direct radio frequency (RF) sampling with recursive filtering method	LEIPOLD, DIRK
10273217	7057540	150	10/17/2002	SIGMA-DELTA (SIGMADELTA) ANALOG-TO-DIGITAL CONVERTER (ADC) STRUCTURE INCORPORATING A DIRECT SAMPLING MIXER	LEIPOLD, DIRK
10280156	Not Issued	41	10/25/2002	Removing close-in interferers through a feedback loop	LEIPOLD, DIRK
10301895	7046098	150	11/22/2002	ALL-DIGITAL FREQUENCY SYNTHESIS WITH CAPACITIVE RE-INTRODUCTION OF DITHERED TUNING	LEIPOLD, DIRK

				INFORMATION	
10302029	Not Issued	41	11/22/2002	All-digital frequency synthesis with DCO gain calculation	LEIPOLD, DIRK
10306655	Not Issued	41	11/27/2002	All-digital frequency synthesis with non-linear differential term for handling frequency perturbations	LEIPOLD, DIRK
10448712	Not Issued	161	05/30/2003	RF differential signal squarer/limiter and balancer with high power supply rejection	LEIPOLD, DIRK
10464957	Not Issued	93	06/19/2003	TYPE-II ALL-DIGITAL PHASE-LOCKED LOOP (PLL)	LEIPOLD, DIRK
10464982	Not Issued	30	06/19/2003	Fine-grained gear-shifting of a digital phase-locked loop (PLL)	LEIPOLD, DIRK
10679792	6791422	150	10/06/2003	FREQUENCY SYNTHESIZER WITH DIGITALLY-CONTROLLED OSCILLATOR	LEIPOLD, DIRK
10712593	Not Issued	41	11/13/2003	Technique for improving antialiasing and adjacent channel interference filtering using cascaded passive IIR filter stages combined with direct sampling and mixing	LEIPOLD, DIRK
10749654	Not Issued	30	12/31/2003	Predistortion calibration in a transceiver assembly	LEIPOLD, DIRK
10758863	Not Issued	30	01/16/2004	Radio frequency built-in self test for quality monitoring of local oscillator and transmitter	LEIPOLD, DIRK
10759911	Not Issued	90	01/16/2004	ON-CHIP RECEIVER SENSITIVITY TEST MECHANISM	LEIPOLD, DIRK
10759912	7035750	150	01/16/2004	ON-CHIP TEST MECHANISM FOR TRANSCEIVER POWER AMPLIFIER AND OSCILLATOR FREQUENCY	LEIPOLD, DIRK
10827577	7023272	150	04/19/2004	MULTI-BAND LOW NOISE AMPLIFIER SYSTEM	LEIPOLD, DIRK
10828386	Not Issued	30	04/20/2004	Image reject filtering in a direct sampling mixer	LEIPOLD, DIRK
10883501	Not Issued	30	06/30/2004	Method and apparatus for crystal drift compensation	LEIPOLD, DIRK
10927879	Not Issued	30	08/27/2004	Digital amplitude modulation	LEIPOLD, DIRK
10966220	Not Issued	61	10/15/2004	Methods and apparatus to control frequency offsets in digitally	LEIPOLD, DIRK

				controlled crystal oscillators	
11009495	Not Issued	41	12/10/2004	System and method for increasing radio frequency (RF)/microwave inductor-capacitor (LC) oscillator frequency tuning range	LEIPOLD, DIRK
11028995	Not Issued	41	01/03/2005	Sampling mixer with asynchronous clock and signal domains	LEIPOLD, DIRK
11062254	Not Issued	30	02/18/2005	Apparatus for and method of noise suppression and dithering to improve resolution quality in a digital RF processor	LEIPOLD, DIRK
11115815	Not Issued	30	04/26/2005	Low noise high isolation transmit buffer gain control mechanism	LEIPOLD, DIRK
11122670	Not Issued	30	05/04/2005	Wireless communications device having type-II all-digital phase-locked loop (PLL)	LEIPOLD, DIRK
11149859	Not Issued	30	06/10/2005	Gain calibration of a digital controlled oscillator	LEIPOLD, DIRK
11178993	Not Issued	71	07/11/2005	Negative contributive offset compensation in a transmit buffer utilizing inverse clocking	LEIPOLD, DIRK
11195060	Not Issued	41	08/02/2005	Efficient pulse amplitude modulation transmit modulation	LEIPOLD, DIRK
11270121	Not Issued	30	11/09/2005	RF transmission leakage mitigator, method of mitigating an RF transmission leakage and CDMA tranceiver employing the same	LEIPOLD, DIRK
11270122	Not Issued	30	11/09/2005	Offset balancer, method of balancing an offset and a wireless receiver employing the balancer and the method	LEIPOLD, DIRK

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Inventor Name Search Result

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Last Name = LEIPOLD
First Name = DIRK

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11294060	Not Issued	30	12/05/2005	System and method for implementing transformer on package substrate	LEIPOLD, DIRK
11339386	Not Issued	20	01/25/2006	Removing close-in interferers through a feedback loop	LEIPOLD, DIRK
11388558	Not Issued	41	03/24/2006	Technique for improving antialiasing and adjacent channel interference filtering using cascaded passive IIR filter stages combined with direct sampling and mixing	LEIPOLD, DIRK
60186251	Not Issued	159	03/01/2000	Hybrid of predictive/closed-loop digital PLL operation	LEIPOLD, DIRK
60186384	Not Issued	159	03/02/2000	Method of 0 mask implantation of buried layer	LEIPOLD, DIRK
60186434	Not Issued	159	03/02/2000	Low resistivity metalization using electroplate	LEIPOLD, DIRK
60186445	Not Issued	159	03/02/2000	Bootstrap direct full-band frequency synthesizer	LEIPOLD, DIRK
60186452	Not Issued	159	03/02/2000	Digitally-controlled vco	LEIPOLD, DIRK
60195926	Not Issued	159	04/10/2000	Multi-tap sub-sample mixer architecture	LEIPOLD, DIRK
60198901	Not Issued	159	04/20/2000	TIME DITHERING METHOD OF THE VCO CONTROL INPUT	LEIPOLD, DIRK
60198907	Not Issued	159	04/20/2000	PLL LOOP COMPENSATION SCHEME FOR THE FREQUENCY/PHASE MODULATION	LEIPOLD, DIRK
60199017	Not Issued	159	04/20/2000	PHASE ERROR INPUT RETIMING METHOD OF A VCO	LEIPOLD, DIRK

60199074	Not Issued	159	04/20/2000	REDUNDANT ARITHMETIC IN A DIGITALLY-CONTROLLED VCO	LEIPOLD, DIRK
60242577	Not Issued	159	10/23/2000	Asynchronous clock retiming method	LEIPOLD, DIRK
60267107	Not Issued	159	02/07/2001	Sequence estimation of the digital fractional phase detector output (coupled with "all-digital phase domain PLL frequency synthesizer")	LEIPOLD, DIRK
60276716	Not Issued	159	03/16/2001	Digitally controlled analog RF filtering with a current steering mixer	LEIPOLD, DIRK
60276727	Not Issued	159	03/16/2001	Direct conversion by sampling integrated received signal	LEIPOLD, DIRK
60286564	Not Issued	159	04/25/2001	Digitally controlled analog RF filtering with a current steering mixer	LEIPOLD, DIRK
60286572	Not Issued	159	04/25/2001	Frequency synthesizer architecture of the digital radio processor (v2.0)	LEIPOLD, DIRK
60286787	Not Issued	159	04/25/2001	Relaxing the readout timing of IFA in MTDSM using extra taps	LEIPOLD, DIRK
60293073	Not Issued	159	05/23/2001	Efficient PAM transmit modulation method (v0.2)	LEIPOLD, DIRK
60312602	Not Issued	159	08/15/2001	Direct RF sampling with recursive filtering method	LEIPOLD, DIRK
60313749	Not Issued	159	08/20/2001	Frequency synthesizer with digitally-controlled oscillator	LEIPOLD, DIRK
60313751	Not Issued	159	08/20/2001	Transmit filter	LEIPOLD, DIRK
60313772	Not Issued	159	08/20/2001	Direct RF sampling with recursive filtering method	LEIPOLD, DIRK
60313905	Not Issued	159	08/21/2001	Power saving circuitry using predictive logic	LEIPOLD, DIRK
60333115	Not Issued	159	11/27/2001	Non-linear differential mode of an all-digital PLL	LEIPOLD, DIRK
60333169	Not Issued	159	11/27/2001	Just-in-time DCO gain calculation	LEIPOLD, DIRK
60341578	Not Issued	159	12/17/2001	Time-deffered calculation of variable phase in the ADPLL synthesizer	LEIPOLD, DIRK
60343673	Not Issued	159	12/29/2001	Current domain sampling in subsampling communication	LEIPOLD, DIRK

				receiver architecture including CDMA despreading	
60343759	Not Issued	159	12/28/2001	Method and apparatus for resampling variable rate data samples for conversion to fixed rate data samples and vice versa in the presence of a high frequency clock	LEIPOLD, DIRK
60343784	Not Issued	159	12/28/2001	Clock noise suppression by stopping operation of the sampling-mode mixer	LEIPOLD, DIRK
60343846	Not Issued	159	12/28/2001	Digital phase-domain PLL frequency synthesizer with differential term for handling frequency perturbations	LEIPOLD, DIRK
60343938	Not Issued	159	12/28/2001	Current domain sampling in subsampling communication receiver architecture including filter realization with current steering	LEIPOLD, DIRK
60344305	Not Issued	159	12/28/2001	Digital phase-domain PLL frequency synthesizer with just-in-time KDCO gain calculation	LEIPOLD, DIRK
60348902	Not Issued	159	10/26/2001	Current steering approach for placing two zeros on folded-over frequencies in decimating FIR filters	LEIPOLD, DIRK
60356620	Not Issued	159	10/25/2001	Sampled domain passive anti-aliasing FIR filter structure with decimation function	LEIPOLD, DIRK
60386290	Not Issued	159	06/05/2002	Digital phase-domain PLL frequendy synthesizer with just-in time KDCO gain calculation	LEIPOLD, DIRK
60389872	Not Issued	159	06/19/2002	Graduated exponential bandwidth shifting of an all-digital PLL	LEIPOLD, DIRK
60411814	Not Issued	159	09/18/2002	Active removal of fractional spurs in an ADPLL	LEIPOLD, DIRK
60441080	Not Issued	159	01/17/2003	Type-II-all-digital PLL in deep-submicron CMOS	LEIPOLD, DIRK
60517119	Not Issued	159	11/03/2003	Smart DCXO frequency offset compensation with temperature sensor and adaptive self calibration algorithm	LEIPOLD, DIRK
60546248	Not Issued	18	02/19/2004	Novel and economic way to increase an RF/microwave LC oscillator frequency tuning range	LEIPOLD, DIRK

60546249	Not Issued	159	02/19/2004	Clock retiming and synchronization method for noise suppression in the digital radio processor	LEIPOLD, DIRK
60577508	Not Issued	159	06/04/2004	Digital method of amplitude modulation for edge	LEIPOLD, DIRK
60583713	Not Issued	159	06/29/2004	Low noise, high isolation gain control scheme for a transmit buffer	LEIPOLD, DIRK
60601586	Not Issued	159	08/12/2004	Low noise, high isolation gain control scheme for a transmit buffer	LEIPOLD, DIRK
60728395	Not Issued	20	10/19/2005	Fab process definition by calculating transistor invert delay period with TDC	LEIPOLD, DIRK
60765678	Not Issued	20	02/06/2006	Power efficient, TRP compliant power control loop using a synchronous high frequency switching powers supply and second harmonic synchronous RF loop-back detection in receiver	LEIPOLD, DIRK
60765679	Not Issued	20	02/06/2006	Package inductor for power efficient, TRP compliant power control loop using a synchronous high frequency switching powers supply and second harmonic synchronous RF loop-back detection in receiver	LEIPOLD, DIRK

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Inventor Name Search Result

Your Search was:

Last Name = STASZEWSKI
First Name = ROBERT

Application#	Patent#	Status	Date Filed	Title	Inventor Name
11178993	Not Issued	71	07/11/2005	Negative contributive offset compensation in a transmit buffer utilizing inverse clocking	STASZEWSKI, ROBERT B.
11195060	Not Issued	41	08/02/2005	Efficient pulse amplitude modulation transmit modulation	STASZEWSKI, ROBERT B.
11203019	Not Issued	30	08/11/2005	Hybrid polar/cartesian digital modulator	STASZEWSKI, ROBERT B.
11203504	Not Issued	160	08/11/2005	Method and apparatus for a fully digital quadrature modulator	STASZEWSKI, ROBERT B.
11274965	Not Issued	41	11/15/2005	Circuit for high-resolution phase detection in a digital RF processor	STASZEWSKI, ROBERT B.
11297524	Not Issued	30	12/07/2005	Transmitter for wireless applications incorporation spectral emission shaping sigma delta modulator	STASZEWSKI, ROBERT B.
11339386	Not Issued	20	01/25/2006	Removing close-in interferers through a feedback loop	STASZEWSKI, ROBERT B.
11382570	Not Issued	30	05/10/2006	FAST HOPPING FREQUENCY SYNTHESIZER USING AN ALL DIGITAL PHASED LOCKED LOOP (ADPLL)	STASZEWSKI, ROBERT B.
11388558	Not Issued	41	03/24/2006	Technique for improving antialiasing and adjacent channel interference filtering using cascaded passive IIR filter stages combined with direct sampling and mixing	STASZEWSKI, ROBERT B.
11460221	Not Issued	19	07/26/2006	HYBRID STOCHASTIC GRADIENT BASED DIGITALLY CONTROLLED OSCILLATOR GAIN KDCO ESTIMATION	STASZEWSKI, ROBERT B.

60186251	Not Issued	159	03/01/2000	Hybrid of predictive/closed-loop digital PLL operation	STASZEWSKI, ROBERT B.
60198907	Not Issued	159	04/20/2000	PLL LOOP COMPENSATION SCHEME FOR THE FREQUENCY/PHASE MODULATION	STASZEWSKI, ROBERT B.
60199074	Not Issued	159	04/20/2000	REDUNDANT ARITHMETIC IN A DIGITALLY-CONTROLLED VCO	STASZEWSKI, ROBERT B.
60242577	Not Issued	159	10/23/2000	Asynchronous clock retiming method	STASZEWSKI, ROBERT B.
60267107	Not Issued	159	02/07/2001	Sequence estimation of the digital fractional phase detector output (coupled with "all-digital phase domain PLL frequency synthesizer")	STASZEWSKI, ROBERT B.
60286572	Not Issued	159	04/25/2001	Frequency synthesizer architecture of the digital radio processor (v2.0)	STASZEWSKI, ROBERT B.
60293073	Not Issued	159	05/23/2001	Efficient PAM transmit modulation method (v0.2)	STASZEWSKI, ROBERT B.
60312602	Not Issued	159	08/15/2001	Direct RF sampling with recursive filtering method	STASZEWSKI, ROBERT B.
60313749	Not Issued	159	08/20/2001	Frequency synthesizer with digitally-controlled oscillator	STASZEWSKI, ROBERT B.
60313751	Not Issued	159	08/20/2001	Transmit filter	STASZEWSKI, ROBERT B.
60313772	Not Issued	159	08/20/2001	Direct RF sampling with recursive filtering method	STASZEWSKI, ROBERT B.
60313905	Not Issued	159	08/21/2001	Power saving circuitry using predictive logic	STASZEWSKI, ROBERT B.
60333115	Not Issued	159	11/27/2001	Non-linear differential mode of an all-digital PLL	STASZEWSKI, ROBERT B.
60333144	Not Issued	159	11/27/2001	Dither elimination technique of a digital sigma-delta modulator for a DCO-based a DPLL frequency synthesizer	STASZEWSKI, ROBERT B.
60333169	Not Issued	159	11/27/2001	Just-in-time DCO gain calculation	STASZEWSKI, ROBERT B.
60341578	Not Issued	159	12/17/2001	Time-deffered calculation of variable phase in the ADPLL synthesizer	STASZEWSKI, ROBERT B.
60343759	Not Issued	159	12/28/2001	Method and apparatus for resampling variable rate data samples for conversion to fixed	STASZEWSKI, ROBERT B.

				rate data samples and vice versa in the presence of a high frequency clock	
60343784	Not Issued	159	12/28/2001	Clock noise suppression by stopping operation of the sampling-mode mixer	STASZEWSKI, ROBERT B.
60343837	Not Issued	159	12/28/2001	Digital phase-domain PLL frequency synthesizer with dithering inside a digital sigma-delta modulator to reduce spurious output tones	STASZEWSKI, ROBERT B.
60343846	Not Issued	159	12/28/2001	Digital phase-domain PLL frequency synthesizer with differential term for handling frequency perturbations	STASZEWSKI, ROBERT B.
60344305	Not Issued	159	12/28/2001	Digital phase-domain PLL frequency synthesizer with just-in-time KDCO gain calculation	STASZEWSKI, ROBERT B.
60348902	Not Issued	159	10/26/2001	Current steering approach for placing two zeros on folded-over frequencies in decimating FIR filters	STASZEWSKI, ROBERT B.
60356620	Not Issued	159	10/25/2001	Sampled domain passive anti-aliasing FIR filter structure with decimation function	STASZEWSKI, ROBERT B.
60386290	Not Issued	159	06/05/2002	Digital phase-domain PLL frequendy synthesizer with just-in time KDCO gain calculation	STASZEWSKI, ROBERT B.
60389872	Not Issued	159	06/19/2002	Graduated exponential bandwidth shifting of an all-digital PLL	STASZEWSKI, ROBERT B.
60411814	Not Issued	159	09/18/2002	Active removal of fractional spurs in an ADPLL	STASZEWSKI, ROBERT B.
60441080	Not Issued	159	01/17/2003	Type-II-all-digital PLL in deep-submicron CMOS	STASZEWSKI, ROBERT B.
60489453	Not Issued	159	07/23/2003	Method of rate conversion together with I-Q mismatch correction and sampler phase adjustment in direct sampling based down-conversion	STASZEWSKI, ROBERT B.
60546249	Not Issued	159	02/19/2004	Clock retiming and synchronization method for noise suppression in the digital radio processor	STASZEWSKI, ROBERT B.
60550919	Not Issued	159	03/05/2004	Crystal drift compensation in a mobile phone	STASZEWSKI, ROBERT B.

60577508	Not Issued	159	06/04/2004	Digital method of amplitude modulation for edge	STASZEWSKI, ROBERT B.
60583713	Not Issued	159	06/29/2004	Low noise, high isolation gain control scheme for a transmit buffer	STASZEWSKI, ROBERT B.
60601374	Not Issued	159	08/12/2004	LMS-based kappaDCO algorithm	STASZEWSKI, ROBERT B.
60601586	Not Issued	159	08/12/2004	Low noise, high isolation gain control scheme for a transmit buffer	STASZEWSKI, ROBERT B.
60601587	Not Issued	159	08/12/2004	Method and apparatus for a fully digital RF transmitter	STASZEWSKI, ROBERT B.
60629829	Not Issued	159	11/18/2004	A circuit for high-resolution phase detection in a digital radio transceiver	STASZEWSKI, ROBERT B.
60634658	Not Issued	159	12/08/2004	Synthesis of sigma delta modulators from arbitrary noise transfer functions	STASZEWSKI, ROBERT B.
60728270	Not Issued	20	10/19/2005	New ADPLL architecture for low-power cellular applications	STASZEWSKI, ROBERT B.
60728274	Not Issued	20	10/19/2005	Continuous reversible gear-shifting based on IIR filtering recursive operation	STASZEWSKI, ROBERT B.
60728395	Not Issued	20	10/19/2005	Fab process definition by calculating transistor invert delay period with TDC	STASZEWSKI, ROBERT B.

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Last Name = STASZEWSKI
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Application#	Patent#	Status	Date Filed	Title	Inventor Name
11464420	Not Issued	19	01/01/0001	Type-II All-Digital Phase-Locked Loop (PLL)	STASZEWSKI, ROBERT
60186445	Not Issued	159	03/02/2000	Bootstrap direct full-band frequency synthesizer	STASZEWSKI, ROBERT
60186452	Not Issued	159	03/02/2000	Digitally-controlled vco	STASZEWSKI, ROBERT
60600147	Not Issued	159	08/10/2004	Methods of hypnosis	STASZEWSKI, ROBERT
60610495	Not Issued	159	09/16/2004	Methods for rapidly inducing medium depth hypnosis, self-hypnosis or meditative states and synergistically incorporating hypnotic suggestions	STASZEWSKI, ROBERT
60198901	Not Issued	159	04/20/2000	TIME DITHERING METHOD OF THE VCO CONTROL INPUT	STASZEWSKI, ROBERT B
60199017	Not Issued	159	04/20/2000	PHASE ERROR INPUT RETIMING METHOD OF A VCO	STASZEWSKI, ROBERT B
09603023	6326851	150	06/26/2000	Digital phase-domain PLL frequency synthesizer	STASZEWSKI, ROBERT B.
09608317	6429693	150	06/30/2000	DIGITAL FRACTIONAL PHASE DETECTOR	STASZEWSKI, ROBERT B.
09679793	6658748	150	10/05/2000	DIGITALLY-CONTROLLED L-C OSCILLATOR	STASZEWSKI, ROBERT B.
09695516	6809598	150	10/24/2000	HYBRID OF PREDICTIVE AND CLOSED-LOOP PHASE-DOMAIN DIGITAL PLL ARCHITECTURE	STASZEWSKI, ROBERT B.
09728180	6851493	150	12/01/2000	DIGITAL PLL WITH GEAR SHIFT	STASZEWSKI, ROBERT B.
09790376	6414555	150	02/22/2001	FREQUENCY SYNTHESIZER	STASZEWSKI,

					ROBERT B.
09828338	6959049	150	04/06/2001	MULTI-TAP, DIGITAL-PULSE-DRIVEN MIXER	STASZEWSKI, ROBERT B.
09838451	6606004	150	04/19/2001	SYSTEM AND METHOD FOR TIME DITHERING A DIGITALLY-CONTROLLED OSCILLATOR TUNING INPUT	STASZEWSKI, ROBERT B.
09967275	6593773	150	09/28/2001	POWER SAVING CIRCUITRY USING PREDICTIVE LOGIC	STASZEWSKI, ROBERT B.
09969307	Not Issued	41	10/02/2001	Method and apparatus for asynchronous clock retiming	STASZEWSKI, ROBERT B.
10001448	Not Issued	41	10/31/2001	Transmit filter	STASZEWSKI, ROBERT B.
10006607	6734741	150	11/30/2001	FREQUENCY SYNTHESIZER WITH DIGITALLY-CONTROLLED OSCILLATOR	STASZEWSKI, ROBERT B.
10008462	7006589	150	11/30/2001	FREQUENCY SYNTHESIZER WITH PHASE RESTART	STASZEWSKI, ROBERT B.
10121761	Not Issued	41	04/12/2002	Sampling mixer with asynchronous clock and signal domains	STASZEWSKI, ROBERT B.
10131523	Not Issued	41	04/24/2002	Digital phase locked loop	STASZEWSKI, ROBERT B.
10147784	7006813	150	05/16/2002	EFFICIENT CHARGE TRANSFER USING A SWITCHED CAPACITOR RESISTOR	STASZEWSKI, ROBERT B.
10154093	6924681	150	05/22/2002	EFFICIENT PULSE AMPLITUDE MODULATION TRANSMIT MODULATION	STASZEWSKI, ROBERT B.
10190867	Not Issued	41	07/08/2002	Direct radio frequency (RF) sampling with recursive filtering method	STASZEWSKI, ROBERT B.
10230041	7076513	150	08/28/2002	METHOD AND ARCHITECTURE FOR CONTROLLING ASYMMETRY OF AN LMS ADAPTATION ALGORITHM THAT CONTROLS FIR FILTER COEFFICIENTS	STASZEWSKI, ROBERT B.
10269349	6856925	150	10/11/2002	ACTIVE REMOVAL OF ALIASING FREQUENCIES IN A DECIMATING	STASZEWSKI, ROBERT B.

				STRUCTURE BY CHANGING A DECIMATION RATIO IN TIME AND SPACE	
10273217	7057540	150	10/17/2002	SIGMA-DELTA (SIGMADELTA) ANALOG-TO-DIGITAL CONVERTER (ADC) STRUCTURE INCORPORATING A DIRECT SAMPLING MIXER	STASZEWSKI, ROBERT B.
10280156	Not Issued	41	10/25/2002	Removing close-in interferers through a feedback loop	STASZEWSKI, ROBERT B.
10301895	7046098	150	11/22/2002	ALL-DIGITAL FREQUENCY SYNTHESIS WITH CAPACITIVE RE-INTRODUCTION OF DITHERED TUNING INFORMATION	STASZEWSKI, ROBERT B.
10302029	Not Issued	41	11/22/2002	All-digital frequency synthesis with DCO gain calculation	STASZEWSKI, ROBERT B.
10306655	Not Issued	41	11/27/2002	All-digital frequency synthesis with non-linear differential term for handling frequency perturbations	STASZEWSKI, ROBERT B.
10464957	Not Issued	93	06/19/2003	TYPE-II ALL-DIGITAL PHASE-LOCKED LOOP (PLL)	STASZEWSKI, ROBERT B.
10464982	Not Issued	30	06/19/2003	Fine-grained gear-shifting of a digital phase-locked loop (PLL)	STASZEWSKI, ROBERT B.
10641235	Not Issued	30	08/14/2003	Method of rate conversion together with I-Q mismatch correction and sampler phase adjustment in direct sampling based down-conversion	STASZEWSKI, ROBERT B.
10679792	6791422	150	10/06/2003	FREQUENCY SYNTHESIZER WITH DIGITALLY-CONTROLLED OSCILLATOR	STASZEWSKI, ROBERT B.
10712593	Not Issued	41	11/13/2003	Technique for improving antialiasing and adjacent channel interference filtering using cascaded passive IIR filter stages combined with direct sampling and mixing	STASZEWSKI, ROBERT B.
10749654	Not Issued	30	12/31/2003	Predistortion calibration in a transceiver assembly	STASZEWSKI, ROBERT B.
10758863	Not	30	01/16/2004	Radio frequency built-in self test	STASZEWSKI,

	Issued			for quality monitoring of local oscillator and transmitter	ROBERT B.
10828386	Not Issued	30	04/20/2004	Image reject filtering in a direct sampling mixer	STASZEWSKI, ROBERT B.
10883501	Not Issued	30	06/30/2004	Method and apparatus for crystal drift compensation	STASZEWSKI, ROBERT B.
10924159	Not Issued	30	08/23/2004	Active removal of aliasing frequencies in a decimating structure by changing a decimation ratio in time and space	STASZEWSKI, ROBERT B.
10924220	Not Issued	61	08/23/2004	Oscillator system, method of providing a resonating signal and a communications system employing the same	STASZEWSKI, ROBERT B.
10924297	Not Issued	30	08/23/2004	Active removal of aliasing frequencies in a decimating structure by changing a decimation ratio in time and space	STASZEWSKI, ROBERT B.
10924303	7103489	150	08/23/2004	ACTIVE REMOVAL OF ALIASING FREQUENCIES IN A DECIMATING STRUCTURE BY CHANGING A DECIMATION RATIO IN TIME AND SPACE	STASZEWSKI, ROBERT B.
11028995	Not Issued	41	01/03/2005	Sampling mixer with asynchronous clock and signal domains	STASZEWSKI, ROBERT B.
11062254	Not Issued	30	02/18/2005	Apparatus for and method of noise suppression and dithering to improve resolution quality in a digital RF processor	STASZEWSKI, ROBERT B.
11115815	Not Issued	30	04/26/2005	Low noise high isolation transmit buffer gain control mechanism	STASZEWSKI, ROBERT B.
11122670	Not Issued	30	05/04/2005	Wireless communications device having type-II all-digital phase-locked loop (PLL)	STASZEWSKI, ROBERT B.
11149859	Not Issued	30	06/10/2005	Gain calibration of a digital controlled oscillator	STASZEWSKI, ROBERT B.

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Last Name = MUHAMMAD
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Application#	Patent#	Status	Date Filed	Title	Inventor Name
09356388	6259385	150	07/16/1999	SYSTEM FOR DATA TRANSCEIVING USING RUN-LENGTH CONSTRAINED CONVOLUTIONAL CODES	MUHAMMAD, KHURRAM
09356768	Not Issued	161	07/16/1999	SYSTEM FOR FAST RADIX-R VITERBI DECODING STRUCTURES	MUHAMMAD, KHURRAM
09678344	Not Issued	149	10/03/2000	Low-area full adder balanced sum and carry delays	MUHAMMAD, KHURRAM
10006607	6734741	150	11/30/2001	FREQUENCY SYNTHESIZER WITH DIGITALLY-CONTROLLED OSCILLATOR	MUHAMMAD, KHURRAM
10099831	7079826	150	03/15/2002	DIGITALLY CONTROLLED ANALOG RF FILTERING IN SUBSAMPLING COMMUNICATION RECEIVER ARCHITECTURE	MUHAMMAD, KHURRAM
10121761	Not Issued	41	04/12/2002	Sampling mixer with asynchronous clock and signal domains	MUHAMMAD, KHURRAM
10132025	7003276	150	04/25/2002	SUBSAMPLING COMMUNICATION RECEIVER ARCHITECTURE WITH GAIN CONTROL AND RSSI GENERATION	MUHAMMAD, KHURRAM
10132436	6963732	150	04/25/2002	SUBSAMPLING COMMUNICATION RECEIVER ARCHITECTURE WITH RELAXED IFA READOUT TIMING	MUHAMMAD, KHURRAM
10132624	Not Issued	41	04/25/2002	Spread spectrum demodulation using a subsampling communication receiver	MUHAMMAD, KHURRAM

				architecture	
10147784	7006813	150	05/16/2002	EFFICIENT CHARGE TRANSFER USING A SWITCHED CAPACITOR RESISTOR	MUHAMMAD, KHURRAM
10190867	Not Issued	41	07/08/2002	Direct radio frequency (RF) sampling with recursive filtering method	MUHAMMAD, KHURRAM
10269349	6856925	150	10/11/2002	ACTIVE REMOVAL OF ALIASING FREQUENCIES IN A DECIMATING STRUCTURE BY CHANGING A DECIMATION RATIO IN TIME AND SPACE	MUHAMMAD, KHURRAM
10273217	7057540	150	10/17/2002	SIGMA-DELTA (SIGMADELTA) ANALOG-TO-DIGITAL CONVERTER (ADC) STRUCTURE INCORPORATING A DIRECT SAMPLING MIXER	MUHAMMAD, KHURRAM
10280156	Not Issued	41	10/25/2002	Removing close-in interferers through a feedback loop	MUHAMMAD, KHURRAM
10464957	Not Issued	93	06/19/2003	TYPE-II ALL-DIGITAL PHASE-LOCKED LOOP (PLL)	MUHAMMAD, KHURRAM
10464982	Not Issued	30	06/19/2003	Fine-grained gear-shifting of a digital phase-locked loop (PLL)	MUHAMMAD, KHURRAM
10641235	Not Issued	30	08/14/2003	Method of rate conversion together with I-Q mismatch correction and sampler phase adjustment in direct sampling based down-conversion	MUHAMMAD, KHURRAM
10679792	6791422	150	10/06/2003	FREQUENCY SYNTHESIZER WITH DIGITALLY-CONTROLLED OSCILLATOR	MUHAMMAD, KHURRAM
10712593	Not Issued	41	11/13/2003	Technique for improving antialiasing and adjacent channel interference filtering using cascaded passive IIR filter stages combined with direct sampling and mixing	MUHAMMAD, KHURRAM
10828386	Not Issued	30	04/20/2004	Image reject filtering in a direct sampling mixer	MUHAMMAD, KHURRAM
10832531	Not Issued	41	04/27/2004	Programmbale loop filter for use with a sigma delta analog-to-	MUHAMMAD, KHURRAM

				digital converter and method of programming the same	
10924159	Not Issued	30	08/23/2004	Active removal of aliasing frequencies in a decimating structure by changing a decimation ratio in time and space	MUHAMMAD, KHURRAM
10924297	Not Issued	30	08/23/2004	Active removal of aliasing frequencies in a decimating structure by changing a decimation ratio in time and space	MUHAMMAD, KHURRAM
10924303	7103489	150	08/23/2004	ACTIVE REMOVAL OF ALIASING FREQUENCIES IN A DECIMATING STRUCTURE BY CHANGING A DECIMATION RATIO IN TIME AND SPACE	MUHAMMAD, KHURRAM
11028995	Not Issued	41	01/03/2005	Sampling mixer with asynchronous clock and signal domains	MUHAMMAD, KHURRAM
11059147	Not Issued	30	02/16/2005	Methods and apparatus to perform signal removal in a low intermediate frequency receiver	MUHAMMAD, KHURRAM
11062254	Not Issued	30	02/18/2005	Apparatus for and method of noise suppression and dithering to improve resolution quality in a digital RF processor	MUHAMMAD, KHURRAM
11122670	Not Issued	30	05/04/2005	Wireless communications device having type-II all-digital phase-locked loop (PLL)	MUHAMMAD, KHURRAM
11159727	Not Issued	30	06/23/2005	Methods and apparatus to compensate for I/Q mismatch in quadrature receivers	MUHAMMAD, KHURRAM
11264442	Not Issued	30	11/01/2005	Method for automatic gain control (AGC) by combining if frequency adjustment with receive path gain adjustment	MUHAMMAD, KHURRAM
11270121	Not Issued	30	11/09/2005	RF transmission leakage mitigator, method of mitigating an RF transmission leakage and CDMA tranceiver employing the same	MUHAMMAD, KHURRAM
11270122	Not Issued	30	11/09/2005	Offset balancer, method of balancing an offset and a wireless receiver employing the	MUHAMMAD, KHURRAM

				balancer and the method	
11339386	Not Issued	20	01/25/2006	Removing close-in interferers through a feedback loop	MUHAMMAD, KHURRAM
11388558	Not Issued	41	03/24/2006	Technique for improving antialiasing and adjacent channel interference filtering using cascaded passive IIR filter stages combined with direct sampling and mixing	MUHAMMAD, KHURRAM
11500083	Not Issued	19	08/07/2006	Method and apparatus to provide digitally controlled crystal oscillators	MUHAMMAD, KHURRAM
60276716	Not Issued	159	03/16/2001	Digitally controlled analog RF filtering with a current steering mixer	MUHAMMAD, KHURRAM
60276727	Not Issued	159	03/16/2001	Direct conversion by sampling integrated received signal	MUHAMMAD, KHURRAM
60286421	Not Issued	159	04/25/2001	Gain control and receive signal strength measurement with direct sampling mixer	MUHAMMAD, KHURRAM
60286564	Not Issued	159	04/25/2001	Digitally controlled analog RF filtering with a current steering mixer	MUHAMMAD, KHURRAM
60286572	Not Issued	159	04/25/2001	Frequency synthesizer architecture of the digital radio processor (v2.0)	MUHAMMAD, KHURRAM
60286626	Not Issued	159	04/25/2001	Clock feed-through reduction by selecting digital sequence in MTDSM	MUHAMMAD, KHURRAM
60286736	Not Issued	159	04/25/2001	Despreading CDMA signals using a multi-tap direct sampler	MUHAMMAD, KHURRAM
60286787	Not Issued	159	04/25/2001	Relaxing the readout timing of IFA in MTDSM using extra taps	MUHAMMAD, KHURRAM
60286788	Not Issued	159	04/25/2001	Differential coefficient scheme in MTDSM	MUHAMMAD, KHURRAM
60312602	Not Issued	159	08/15/2001	Direct RF sampling with recursive filtering method	MUHAMMAD, KHURRAM
60313749	Not Issued	159	08/20/2001	Frequency synthesizer with digitally-controlled oscillator	MUHAMMAD, KHURRAM
60313772	Not Issued	159	08/20/2001	Direct RF sampling with recursive filtering method	MUHAMMAD, KHURRAM
60343653	Not Issued	159	12/28/2001	Current domain sampling in subsampling communication receiver architecture with relaxed	MUHAMMAD, KHURRAM

				IFA readout timing	
60343673	Not Issued	159	12/29/2001	Current domain sampling in subsampling communication receiver architecture including CDMA despreading	MUHAMMAD, KHURRAM
60343759	Not Issued	159	12/28/2001	Method and apparatus for resampling variable rate data samples for conversion to fixed rate data samples and vice versa in the presence of a high frequency clock	MUHAMMAD, KHURRAM

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